LOW-POWER 16-CHANNEL CONSTANT-CURRENT LED SINK DRIVER

FEATURES

- **16 Constant-Current Output Channels**
- **Constant Output Current Invariant to Load Voltage Change**
- **Excellent Output Current Accuracy:**
  - **Between Channels: < ±4% (Max)**
  - **Between ICs: < ±6% (Max)**
- **Constant Output Current Range: 3 mA to 45 mA**
- **Output Current Adjusted By External Resistor**
- **Fast Response of Output Current, $\overline{OE}$ (Min): 100 ns**
- **30-MHz Clock Frequency**
- **Schmitt-Trigger Inputs**
- **3.3-V to 5-V Supply Voltage**
- **Thermal Shutdown for Overtemperature Protection**
- **ESD Performance: 1-kV HBM**

APPLICATIONS

- **Gaming Machine / Entertainment**
- **General LED Applications**
- **LED Display Systems**
- **Signs LED Lighting**
- **White Goods**

DESCRIPTION/ORDERING INFORMATION

The TLC5925 is designed for LED displays and LED lighting applications. The TLC5925 contains a 16-bit shift register and data latches, which convert serial input data into parallel output format. At the TLC5925 output stage, 16 regulated-current ports provide uniform and constant current for driving LEDs within a wide range of VF variations. Used in system design for LED display applications (e.g., LED panels), the TLC5925 provides great flexibility and device performance. Users can adjust the output current from 3 mA to 45 mA through an external resistor, R_{ext}, which gives flexibility in controlling the light intensity of LEDs. TLC5925 is designed for up to 17 V at the output port. The high clock frequency, 30 MHz, also satisfies the system requirements of high-volume data transmission.

The serial data is transferred into TLC5925 via SDI, shifted in the shift register, and transferred out via SDO. LE can latch the serial data in the shift register to the output latch. $\overline{OE}$ enables the output drivers to sink current.

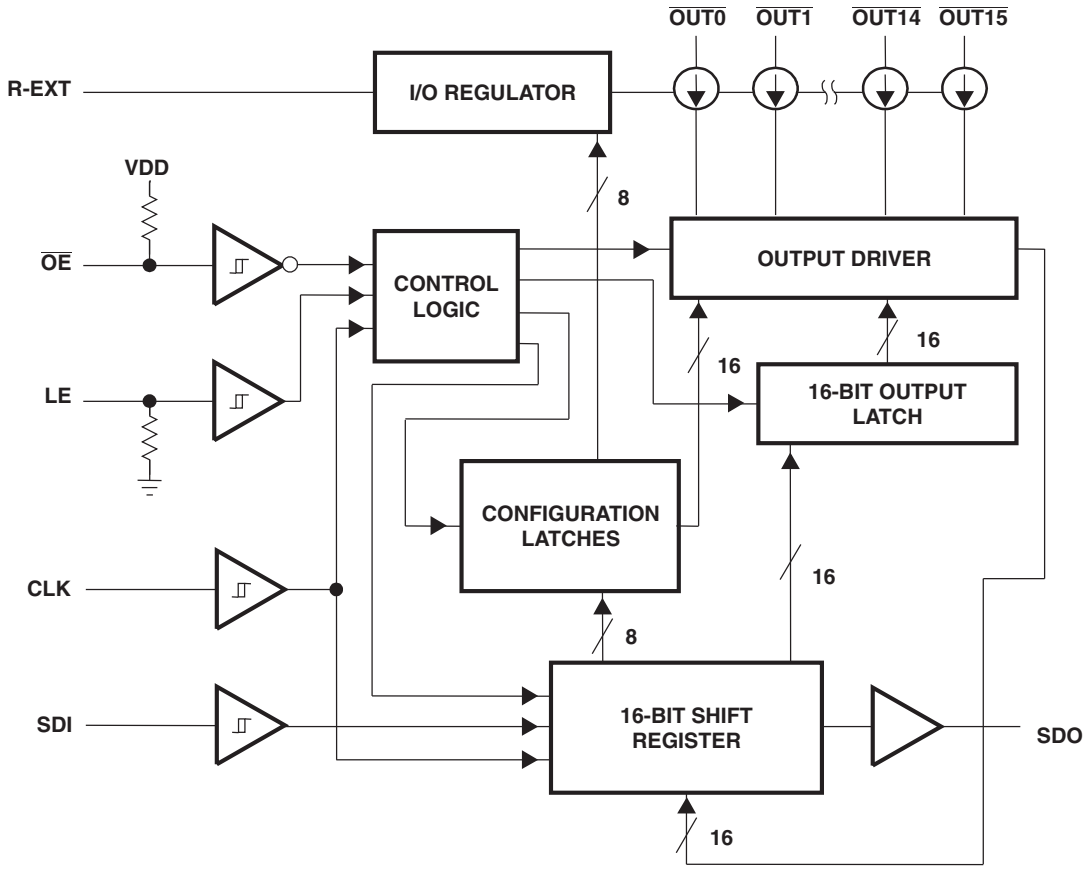
ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PW	Reel of 2000	TLC5925IPWR	Y5925
	W-SOIC – DW	Reel of 2000	TLC5925IDWR	PREVIEW
	SSOP – DBQ	Reel of 2000	TLC5925IDBQR	TLC5925I

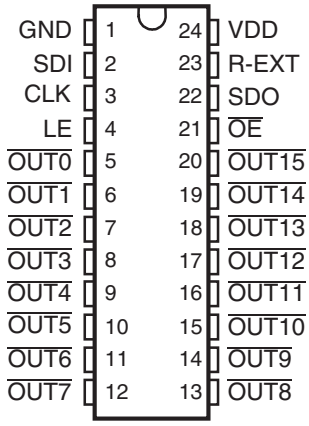
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

BLOCK DIAGRAM



DBQ, DW, OR PWP PACKAGE
(TOP VIEW)



Terminal Descriptions

TERMINAL NAME	DESCRIPTION
CLK	Clock input for data shift on rising edge
GND	Ground for control logic and current sink
LE	Data strobe input Serial data is transferred to the respective latch when LE is high. The data is latched when LE goes low. LE has an internal pull-down resistor.
$\overline{OE}$	Output enable When $\overline{OE}$ is active (low), the output drivers are enabled. When $\overline{OE}$ is high, all output drivers are turned OFF (blanked). $\overline{OE}$ has an internal pullup resistor.
$\overline{OUT0}$–$\overline{OUT15}$	Constant-current outputs
R-EXT	Input used to connect an external resistor (R_{ext}) for setting output currents
SDI	Serial-data input to the Shift register
SDO	Serial-data output to the following SDI of next driver IC or to the microcontroller
VDD	Supply voltage

Timing Diagram

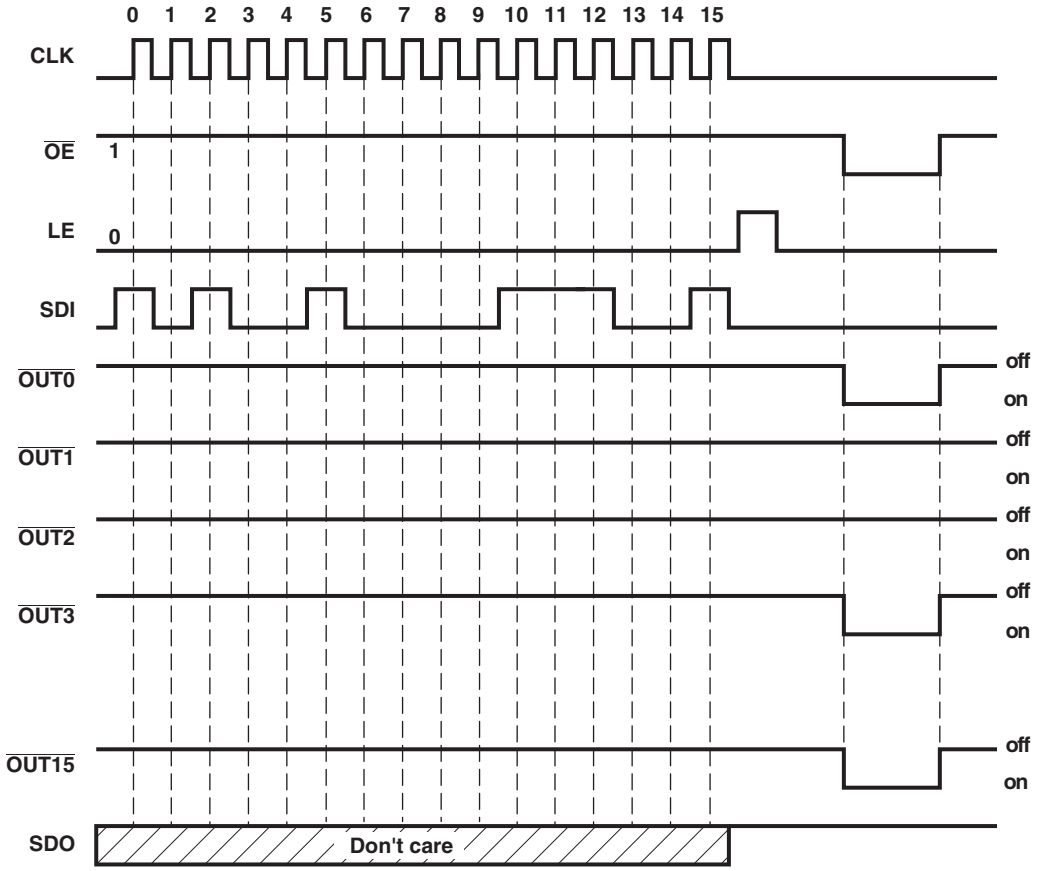


Figure 1. Timing Diagram

Truth Table in Normal Operation

CLK	LE	$\overline{OE}$	SDI	$\overline{OUT0}$...$\overline{OUT15}$...$\overline{OUT15}$	SDO
↑	H	L	Dn	Dn...Dn – 7...Dn – 15	Dn – 15
↑	L	L	Dn + 1	No change	Dn – 14
↑	H	L	Dn + 2	Dn + 2...Dn – 5...Dn – 13	Dn – 13
↓	X	L	Dn + 3	Dn + 2...Dn – 5...Dn – 13	Dn – 13
↓	X	H	Dn + 3	off	Dn – 13

Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{DD}	Supply voltage	0	7	V
V_I	Input voltage	–0.4	V_{DD} + 0.4	V
V_O	Output voltage	–0.5	20	V
I_{OUT}	Output current		45	mA
I_{GND}	GND terminal current		750	mA
T_A	Free-air operating temperature range	–40	125	°C
T_J	Operating junction temperature range	–40	150	°C
T_{stg}	Storage temperature range	–55	150	°C

Power Dissipation and Thermal Impedance

				MIN	MAX	UNIT
P_D	Power dissipation	Mounted on JEDEC 4-layer board (JESD 51-7), No airflow, T_A = 25°C, T_J = 125°C	DBQ package		1.6	W
			DW package		2.2	
			PW package		1.1	
θ_{JA}	Thermal impedance, junction to free air	Mounted on JEDEC 1-layer board (JESD 51-3), No airflow	DBQ package		99.8	°C/W
			DW package		80.5	
			PW package		118.8	
		Mounted on JEDEC 4-layer board (JESD 51-7), No airflow	DBQ package		61.0	
			DW package		45.5	
			PW package		87.9	

Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		TEST CONDITIONS		MIN	MAX	UNIT
V_{DD}	Supply voltage			3	5.5	V
V_O	Output voltage	$\overline{OUT0}$ to $\overline{OUT15}$			17	V
I_O	Output current	DC test circuit	$V_O \geq 0.6$ V	3		mA
			$V_O \geq 1$ V		45	
I_{OH}	High-level output current	SDO		–1		mA
I_{OL}	Low-level output current	SDO		1		mA
V_{IH}	High-level input voltage	CLK, $\overline{OE}$, LE, and SDI		0.7 × V_{DD}	V_{DD}	V
V_{IL}	Low-level input voltage	CLK, $\overline{OE}$, LE, and SDI		GND	0.3 × V_{DD}	V
t_R	Rise Time	CLK			500	ns
t_F	Fall Time	CLK			500	ns

Recommended Timing

V_{DD} = 3 V to 5.5 V (unless otherwise noted)

		TEST CONDITIONS	MIN	MAX	UNIT
$t_{w(L)}$	LE pulse duration		15		ns
$t_{w(CLK)}$	CLK pulse duration		15		ns
$t_{w(OE)}$	$\overline{OE}$ pulse duration		300		ns
$t_{su(D)}$	Setup time for SDI		3		ns
$t_{h(D)}$	Hold time for SDI		2		ns
$t_{su(L)}$	Setup time for LE		5		ns
$t_{h(L)}$	Hold time for LE		5		ns
f_{CLK}	Clock frequency	Cascade operation		30	MHz

Electrical Characteristics

V_{DD} = 3 V, T_J = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{DD}	Input voltage			3		5.5	V
V_O	Output voltage					17	V
I_O	Output current	$V_O \geq 0.6$ V		3			mA
		$V_O \geq 1$ V				45	
I_{OH}	High-level output current, source			-1			mA
I_{OL}	Low-level output current, sink			1			
V_{IH}	High-level input voltage			0.7 × V_{DD}		V_{DD}	V
V_{IL}	Low-level input voltage			GND		0.3 × V_{DD}	
I_{leak}	Output leakage current	V_{OH} = 17 V	T_J = 25°C			0.5	µA
			T_J = 125°C			2	
V_{OH}	High-level output voltage	SDO, I_{OL} = –1 mA		V_{DD} – 0.4			V
V_{OL}	Low-level output voltage	SDO, I_{OH} = 1 mA				0.4	V
$I_{O(1)}$	Output current 1	V_{OUT} = 0.6 V, R_{ext} = 1680 Ω			13		mA
	Output current error, die-die	I_{OL} = 13 mA, V_O = 0.6 V, R_{ext} = 1680 Ω, T_J = 25°C			±3	±6	%
	Output current error, channel-to-channel	I_{OL} = 13 mA, V_O = 0.6 V, R_{ext} = 1680 Ω, T_J = 25°C			±1.5	±4	%
$I_{O(2)}$	Output current 2	V_O = 0.8 V, R_{ext} = 840 Ω			26		mA
	Output current error, die-die	I_{OL} = 26 mA, V_O = 0.8 V, R_{ext} = 840 Ω, T_J = 25°C			±3	±6	%
	Output current error, channel-to-channel	I_{OL} = 26 mA, V_O = 0.8 V, R_{ext} = 840 Ω, T_J = 25°C			±1.5	±4	%
I_{OUT} vs V_{OUT}	Output current vs output voltage regulation	V_O = 1 V to 3 V, I_O = 13 mA			±0.1		%/V
		V_{DD} = 3.0 V to 5.5 V, I_O = 13 mA to 45 mA			±1		
	Pullup resistance	$\overline{OE}$			500		kΩ
	Pulldown resistance	LE			500		kΩ
T_{sd}	Overtemperature shutdown(1)			150	175	200	°C
T_{hys}	Restart temperature hysteresis				15		°C
I_{DD}	Supply current	R_{ext} = Open			7	10	mA
		R_{ext} = 1680 Ω			9	12	
		R_{ext} = 840 Ω			11	13	
C_{IN}	Input capacitance	V_I = V_{DD} or GND, CLK, SDI, SDO, $\overline{OE}$				10	pF

(1) Specified by design

Electrical Characteristics

V_{DD} = 5.5 V, T_J = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{DD}	Input voltage			3		5.5	V
V_O	Output voltage					17	V
I_O	Output current	$V_O \geq 0.6$ V		3			mA
		$V_O \geq 1$ V				45	
I_{OH}	High-level output current, source			-1			mA
I_{OL}	Low-level output current, sink			1			
V_{IH}	High-level input voltage			0.7 × V_{DD}		V_{DD}	V
V_{IL}	Low-level input voltage			GND		03 × V_{DD}	
I_{leak}	Output leakage current	V_{OH} = 17 V	T_J = 25°C			0.5	µA
			T_J = 125°C			2	
V_{OH}	High-level output voltage	SDO, I_{OL} = –1 mA		V_{DD} – 0.4			V
V_{OL}	Low-level output voltage	SDO, I_{OH} = 1 mA				0.4	V
$I_{O(1)}$	Output current 1	V_{OUT} = 0.6 V, R_{ext} = 1680 Ω			13		mA
	Output current error, die-die	I_{OL} = 13 mA, V_O = 0.6 V, R_{ext} = 1680 Ω, T_J = 25°C			±3	±6	%
	Output current error, channel-to-channel	I_{OL} = 13 mA, V_O = 0.6 V, R_{ext} = 1680 Ω, T_J = 25°C			±1.5	±4	%
$I_{O(2)}$	Output current 2	V_O = 0.8 V, R_{ext} = 840 Ω			26		mA
	Output current error, die-die	I_{OL} = 26 mA, V_O = 0.8 V, R_{ext} = 840 Ω, T_J = 25°C			±3	±6	%
	Output current error, channel-to-channel	I_{OL} = 26 mA, V_O = 0.8 V, R_{ext} = 840 Ω, T_J = 25°C			±1.5	±4	%
I_{OUT} vs V_{OUT}	Output current vs output voltage regulation	V_O = 1 V to 3 V , I_O = 26 mA			±0.1		%/V
		V_{DD} = 3.0 V to 5.5 V, I_O = 13 mA to 45 mA			±1		
	Pullup resistance	$\overline{OE}$			500		kΩ
	Pulldown resistance	LE			500		kΩ
T_{sd}	Overtemperature shutdown(1)			150	175	200	°C
T_{hys}	Restart temperature hysteresis				15		°C
I_{DD}	Supply current	R_{ext} = Open			9	11	mA
		R_{ext} = 1680 Ω			12	14	
		R_{ext} = 840 Ω			14	16	
C_{IN}	Input capacitance	$V_I = V_{DD}$ or GND, CLK, SDI, SDO, $\overline{OE}$				10	pF

(1) Specified by design

Switching Characteristics

V_{DD} = 3 V, T_J = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH1}	Low-to-high propagation delay time, CLK to $\overline{OUTn}$	$V_{IH} = V_{DD}$, V_{IL} = GND, R_{ext} = 840 Ω, V_L = 4 V, R_L = 88 Ω, C_L = 10 pF	30	45	60	ns
t_{PLH2}	Low-to-high propagation delay time, LE to $\overline{OUTn}$		30	45	60	ns
t_{PLH3}	Low-to-high propagation delay time, $\overline{OE}$ to $\overline{OUTn}$		30	45	60	ns
t_{PLH4}	Low-to-high propagation delay time, CLK to SDO			30	40	ns
t_{PHL1}	High-to-low propagation delay time, CLK to $\overline{OUTn}$		40	65	100	ns
t_{PHL2}	High-to-low propagation delay time, LE to $\overline{OUTn}$		40	65	100	ns
t_{PHL3}	High-to-low propagation delay time, $\overline{OE}$ to $\overline{OUTn}$		40	65	100	ns
t_{PHL4}	High-to-low propagation delay time, CLK to SDO			30	40	ns
$t_{w(CLK)}$	Pulse duration, CLK		15			ns
$t_{w(L)}$	Pulse duration LE		15			ns
$t_{w(OE)}$	Pulse duration, $\overline{OE}$		300			ns
$t_{h(D)}$	Hold time, SDI		2			ns
$t_{su(D)}$	Setup time, SDI		3			ns
$t_{h(L)}$	Hold time, LE		5			ns
$t_{su(L)}$	Setup time, LE		5			ns
t_r	Rise time, CLK(1)				500	ns
t_f	Fall time, CLK(1)				500	ns
t_{or}	Rise time, outputs (off)		35	50	70	ns
t_{of}	Rise time, outputs (on)		15	50	120	ns
f_{CLK}	Clock frequency	Cascade operation			30	MHz

(1) If the devices are connected in cascade and t_r or t_f is large, it may be critical to achieve the timing required for data transfer between two cascaded devices.

Switching Characteristics

V_{DD} = 5.5 V, T_J = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH1}	Low-to-high propagation delay time, CLK to $\overline{OUTn}$	$V_{IH} = V_{DD}$, V_{IL} = GND, R_{ext} = 840 Ω, V_L = 4 V, R_L = 88 Ω, C_L = 10 pF	20	35	55	ns
t_{PLH2}	Low-to-high propagation delay time, LE to $\overline{OUTn}$		20	35	55	ns
t_{PLH3}	Low-to-high propagation delay time, $\overline{OE}$ to $\overline{OUTn}$		20	35	55	ns
t_{PLH4}	Low-to-high propagation delay time, CLK to SDO			20	30	ns
t_{PHL1}	High-to-low propagation delay time, CLK to $\overline{OUTn}$		15	28	42	ns
t_{PHL2}	High-to-low propagation delay time, LE to $\overline{OUTn}$		15	28	42	ns
t_{PHL3}	High-to-low propagation delay time, $\overline{OE}$ to $\overline{OUTn}$		15	28	42	ns
t_{PHL4}	High-to-low propagation delay time, CLK to SDO			20	30	ns
$t_{w(CLK)}$	Pulse duration, CLK		10			ns
$t_{w(L)}$	Pulse duration LE		10			ns
$t_{w(OE)}$	Pulse duration, $\overline{OE}$		200			ns
$t_{h(D)}$	Hold time, SDI		2			ns
$t_{su(D)}$	Setup time, SDI		3			ns
$t_{h(L)}$	Hold time, LE		5			ns
$t_{su(L)}$	Setup time, LE		5			ns
t_r	Rise time, CLK(1)				500	ns
t_f	Fall time, CLK(1)				500	ns
t_{or}	Rise time, outputs (off)		25	45	65	ns
t_{of}	Rise time, outputs (on)		7	12	20	ns
f_{CLK}	Clock frequency	Cascade operation			30	MHz

(1) If the devices are connected in cascade and t_r or t_f is large, it may be critical to achieve the timing required for data transfer between two cascaded devices.

PARAMETER MEASUREMENT INFORMATION

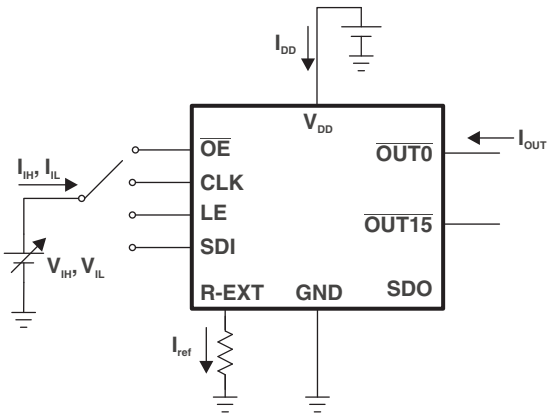


Figure 2. Test Circuit for Electrical Characteristics

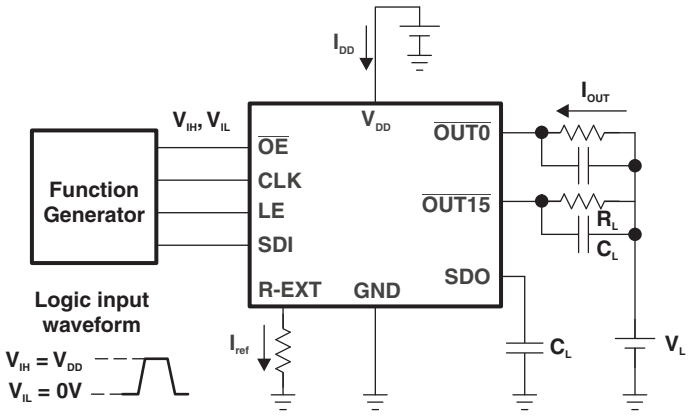


Figure 3. Test Circuit for Switching Characteristics

PARAMETER MEASUREMENT INFORMATION (continued)

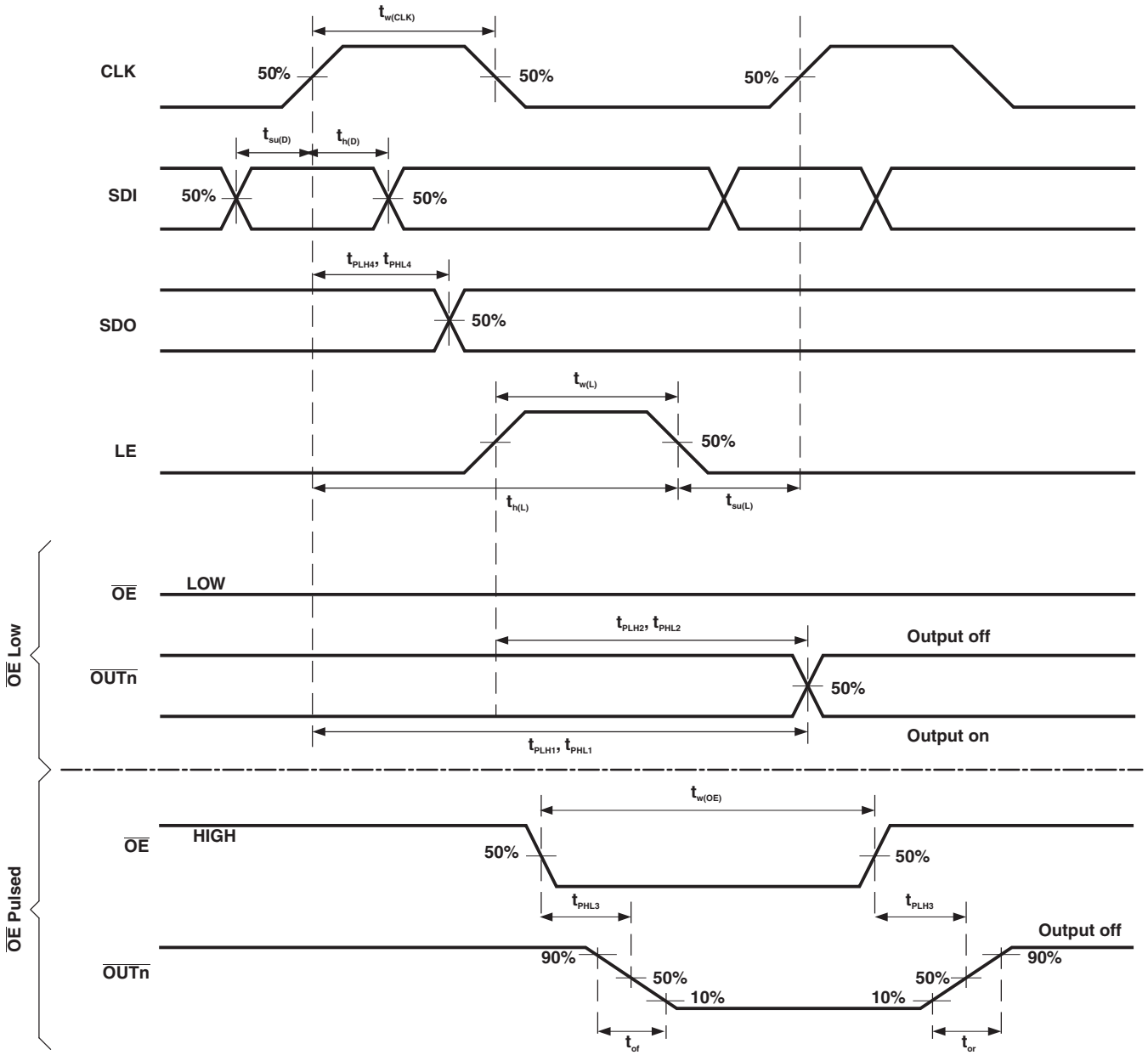


Figure 4. Normal Mode Timing Waveforms

APPLICATION INFORMATION

Operating Principles

Constant Current

In LED display applications, TLC5925 provides nearly no current variations from channel to channel and from IC to IC. While $I_{OUT} \leq 45$ mA, the maximum current skew between channels is less than ±5% and between ICs is less than ±6%.

Adjusting Output Current

TLC5925 sets I_{OUT} based on the external resistor R_{ext}. Users can follow the below formulas to calculate the target output current $I_{OUT,target}$ in the saturation region:

$I_{OUT,target} = (1.21\ V / R_{ext}) \times 18$, where R_{ext} is the external resistance connected between R-EXT and GND.

Therefore, the default current is approximately 26 mA at 840 Ω and 13 mA at 1680 Ω. The default relationship after power on between $I_{OUT,target}$ and R_{ext} is shown in Figure 5.

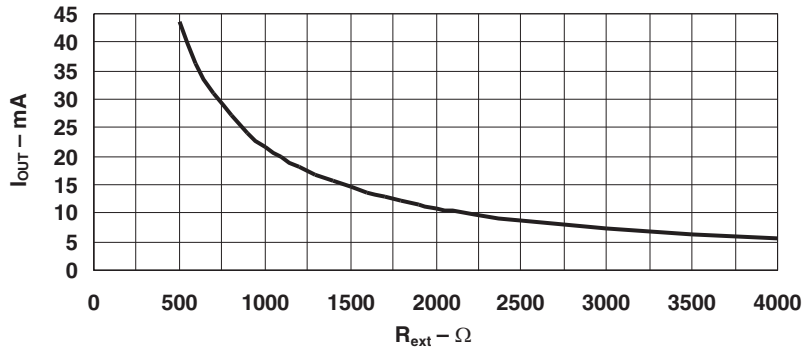


Figure 5. Default Relationship Curve Between $I_{OUT,target}$ and R_{ext} After Power Up

Propagation Delay Times

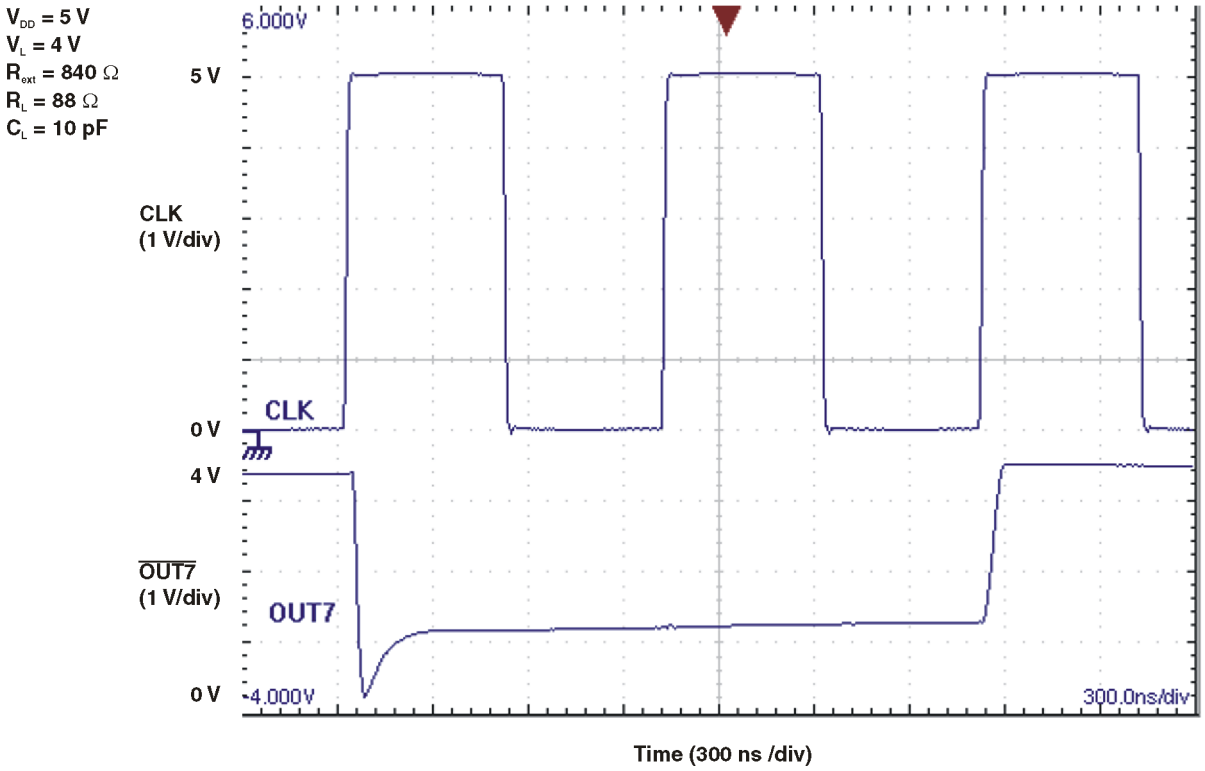


Figure 6. CLK to $\overline{OUT7}$

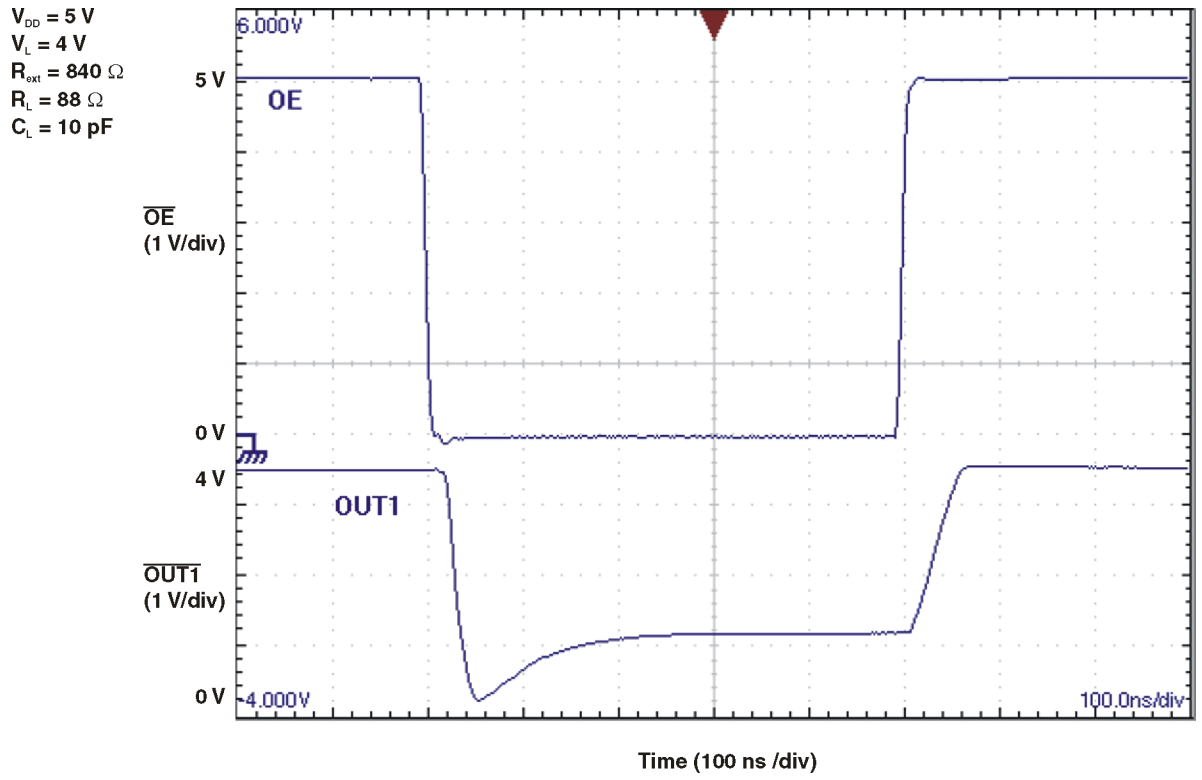


Figure 7. $\overline{OE}$ to $\overline{OUT1}$

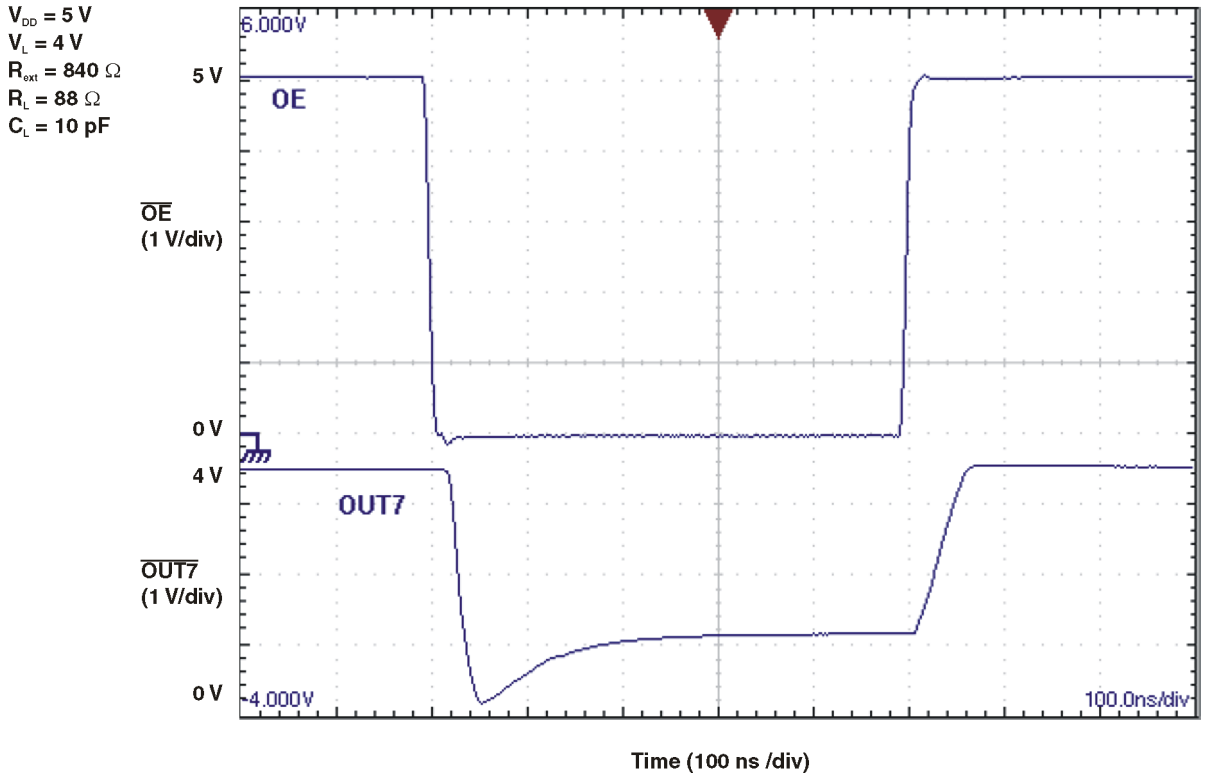


Figure 8. $\overline{OE}$ to $\overline{OUT7}$

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TLC5925IDBQR	ACTIVE	SSOP/ QSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TLC5925IDBQRG4	ACTIVE	SSOP/ QSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TLC5925IDWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC5925IDWRG4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC5925IPWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC5925IPWRG4	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

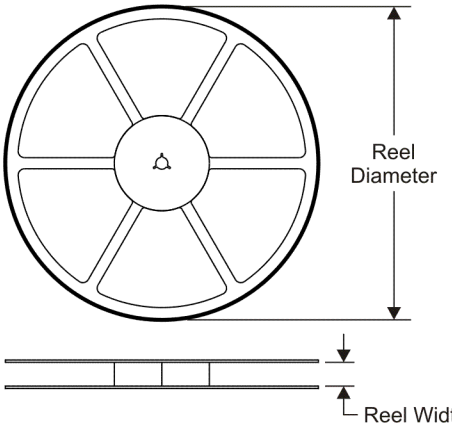
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

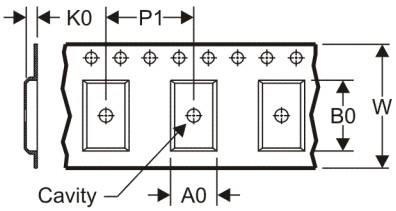
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

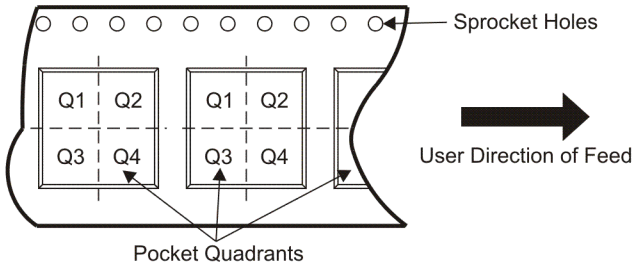


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

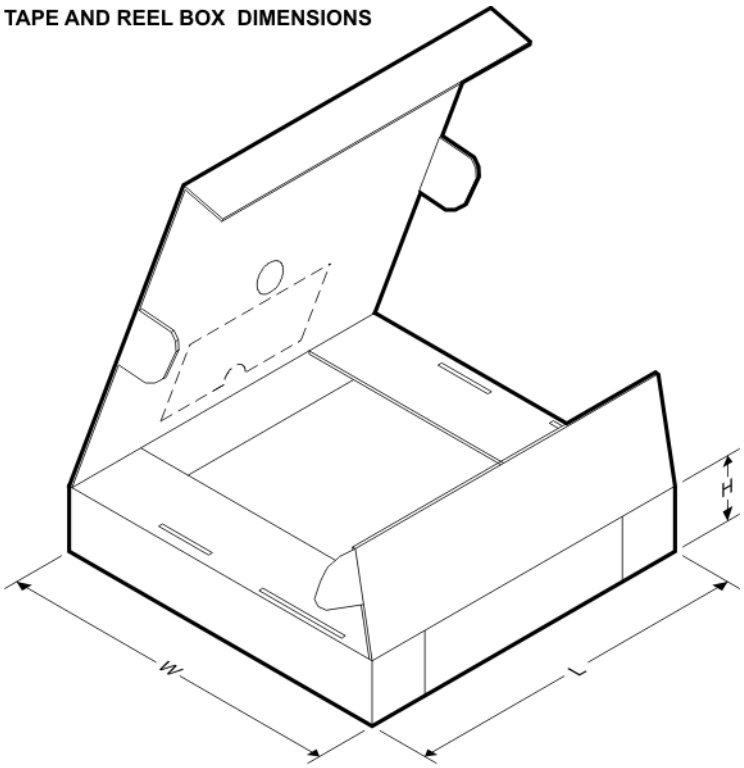
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC5925IDBQR	SSOP/ QSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC5925IPWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

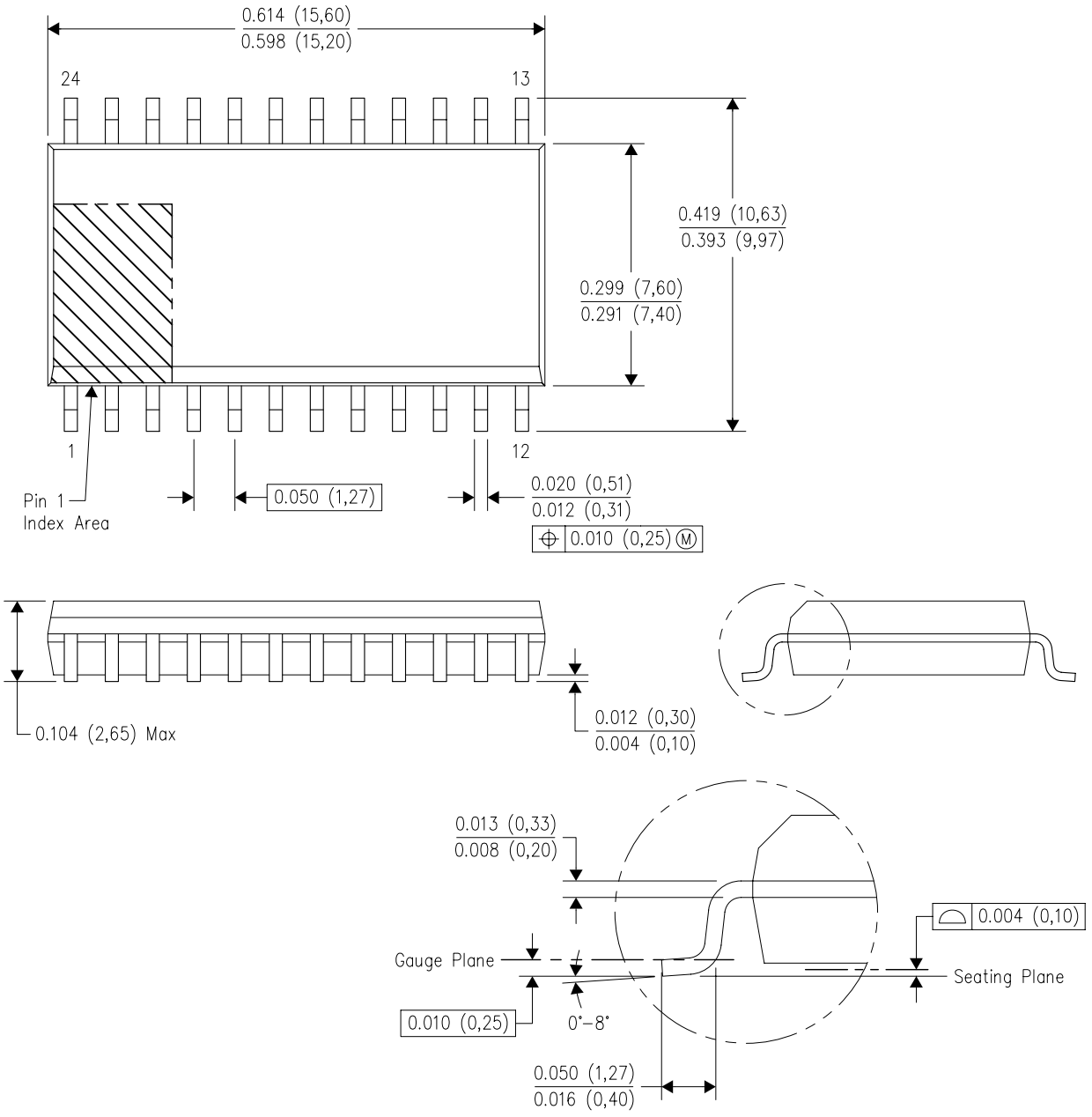
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

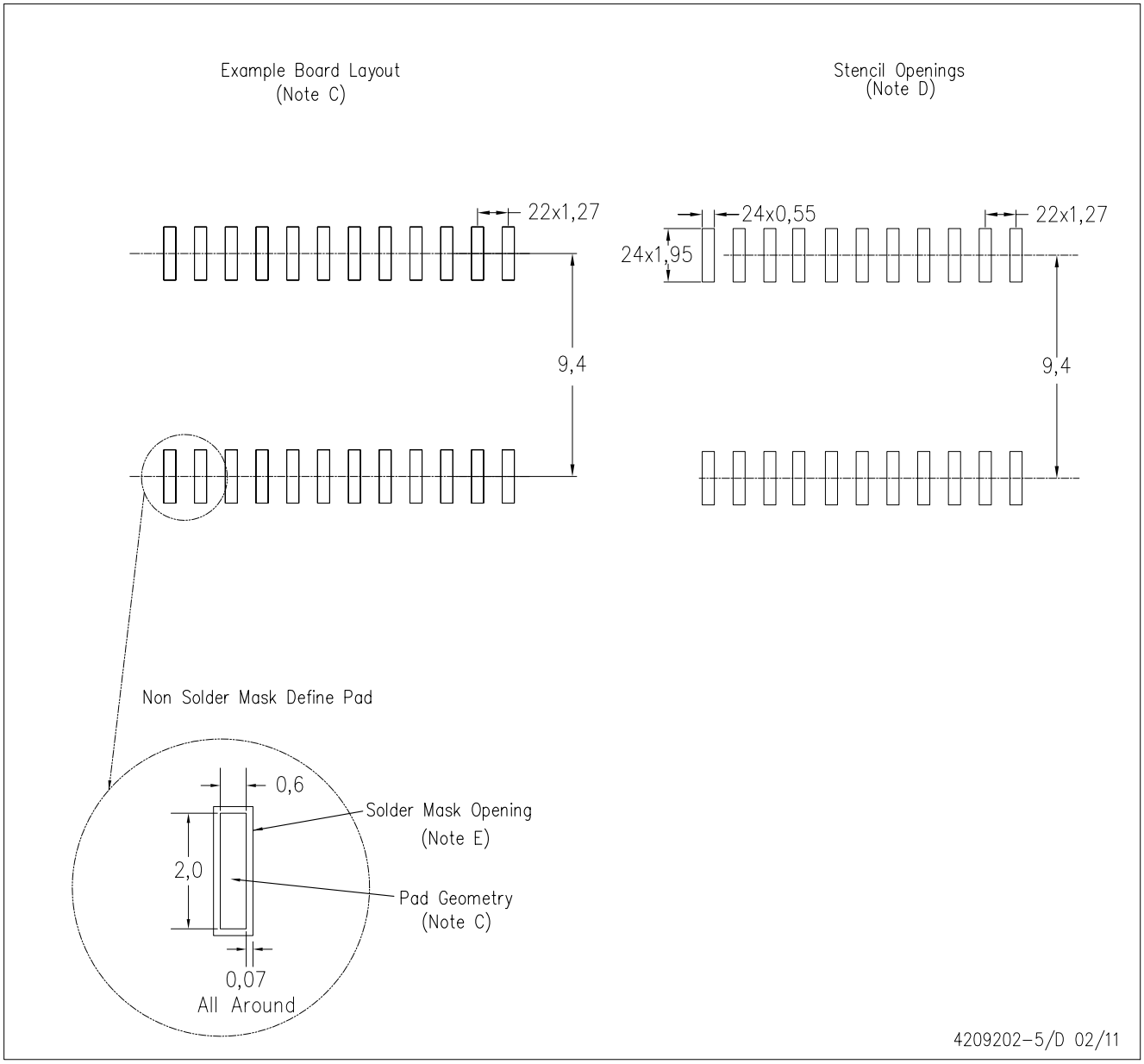
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC5925IDBQR	SSOP/QSOP	DBQ	24	2500	346.0	346.0	33.0
TLC5925IPWR	TSSOP	PW	24	2000	346.0	346.0	33.0

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE



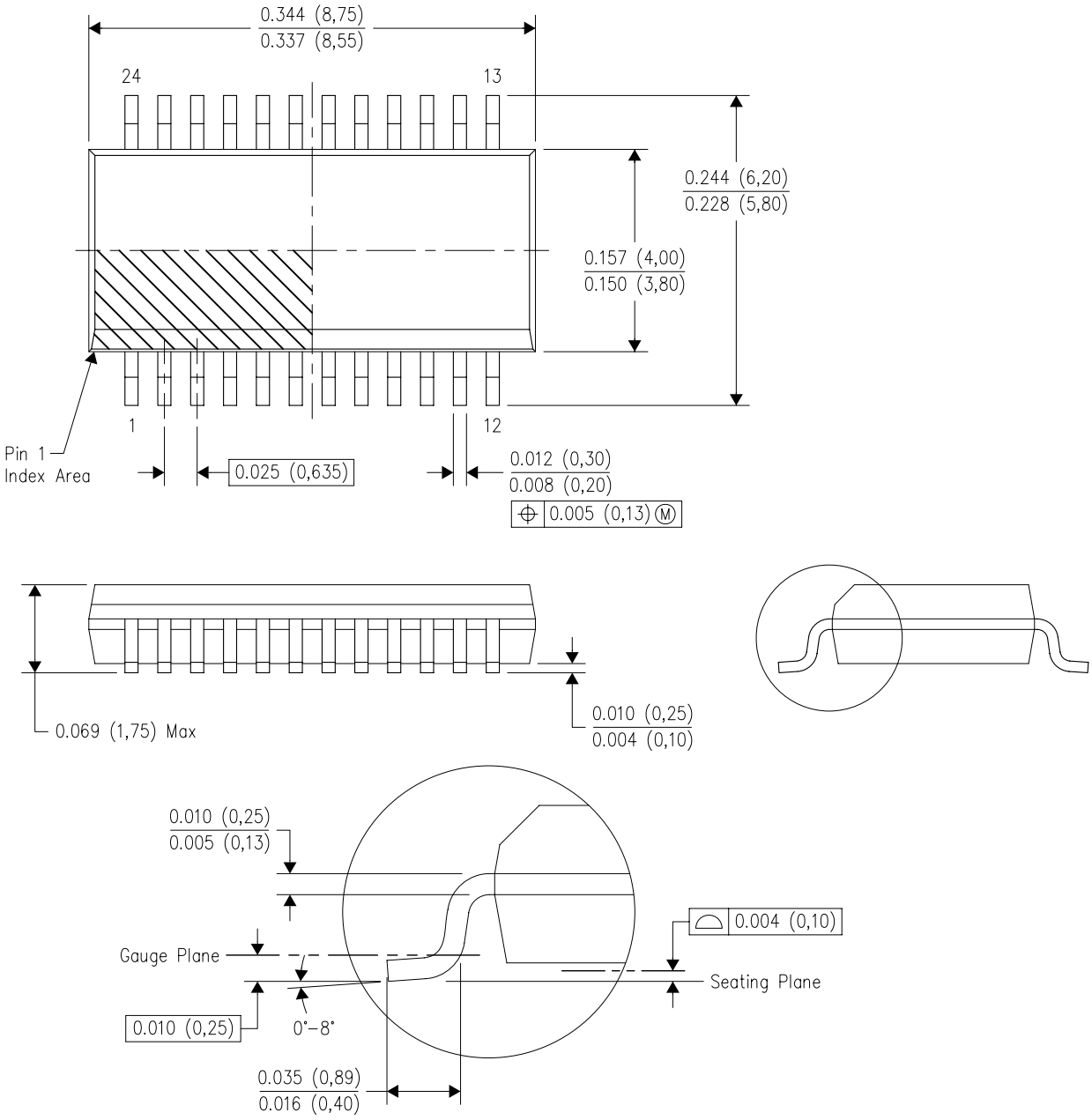
NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AD.

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE



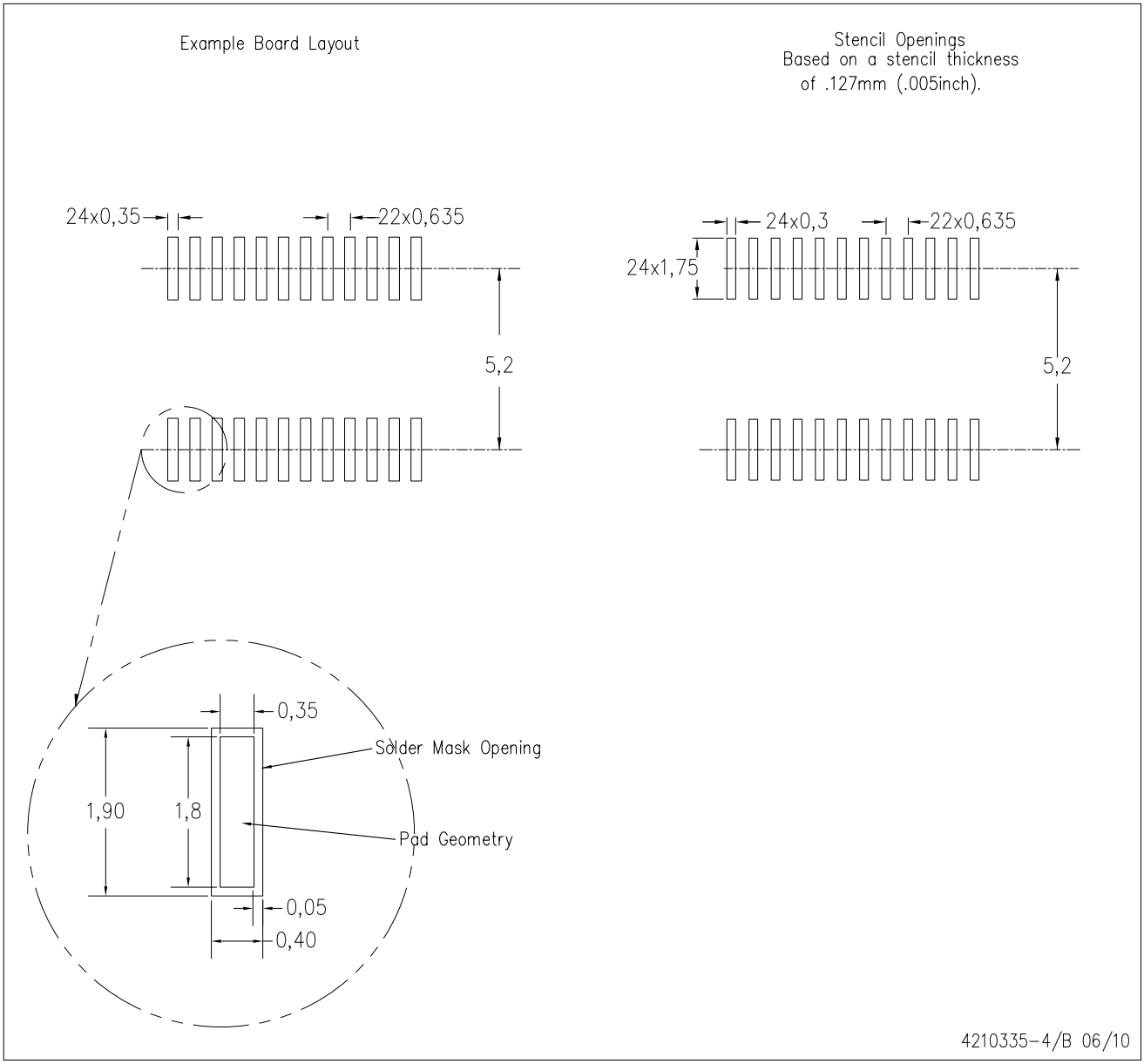
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DBQ (R–PDSO–G24) PLASTIC SMALL–OUTLINE PACKAGE



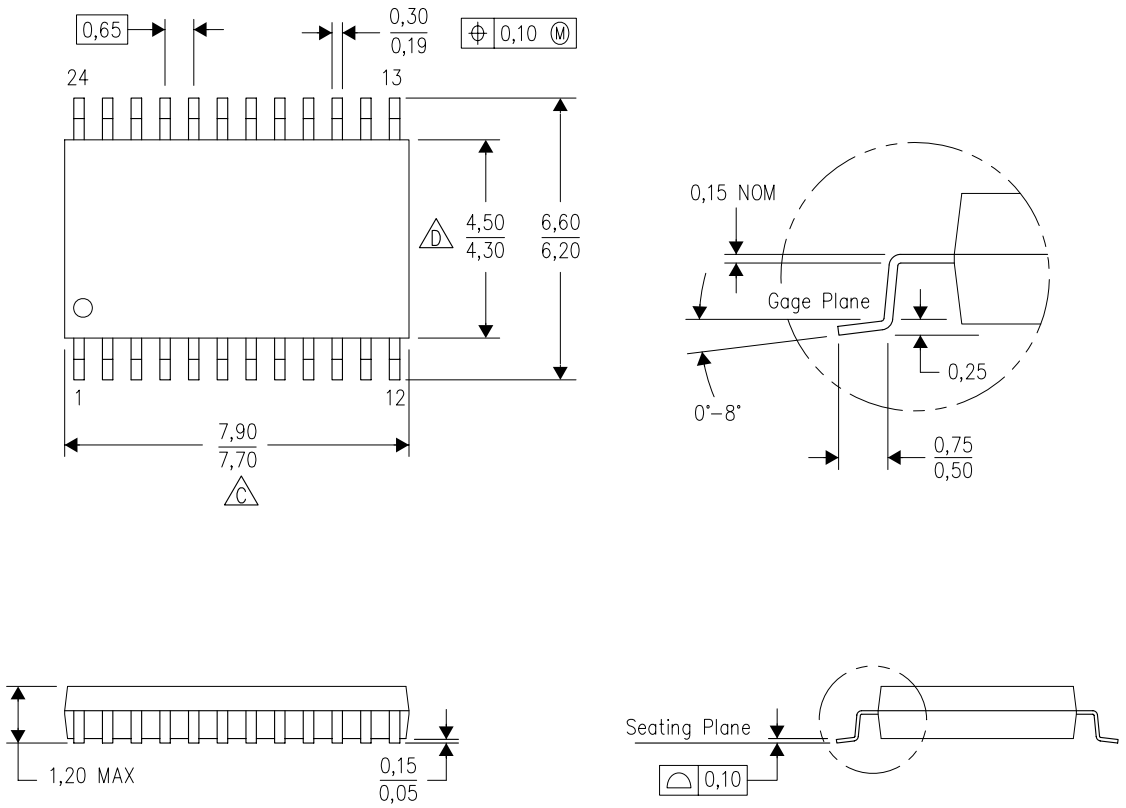
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
D. Falls within JEDEC MO–137 variation AE.

DBQ (R–PDSO–G24) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

PW (R–PDSO–G24) PLASTIC SMALL OUTLINE



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NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

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