HARRIS SEMICONDUCTOR

RFP30N06LE, RF1S30N06LE, RF1S30N06LESM

30A, 60V, ESD Rated, Avalanche Rated, Logic Level N-Channel Enhancement-Mode Power MOSFETs

July 1995

Features

- **30A, 60V**
- **$r_{DS(ON)}$ = 0.047Ω**
- **2kV ESD Protected**
- ***Temperature Compensating* PSPICE Model**
- **Peak Current vs Pulse Width Curve**
- **UIS Rating Curve**

Description

The RFP30N06LE, RF1S30N06LE and RF1S30N06LESM are N-Channel power MOSFETs manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers and relay drivers. These transistors can be operated directly from integrated circuits.

These transistors incorporate ESD protection and are designed to withstand 2kV (Human Body Model) of ESD.

PACKAGE AVAILABILITY

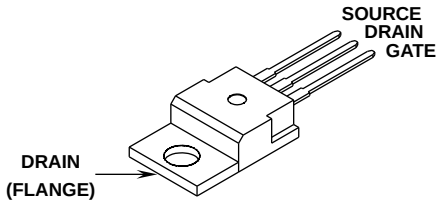
PART NUMBER	PACKAGE	BRAND
RFP30N06LE	TO-220AB	F30N06LE
RF1S30N06LE	TO-262AA	1S30N06L
RF1S30N06LESM	TO-263AB	1S30N06L

NOTE: When ordering use the entire part number. Add suffix, 9A, to obtain the TO-263 variant in tape and reel i.e. RF1S30N06LESM9A.

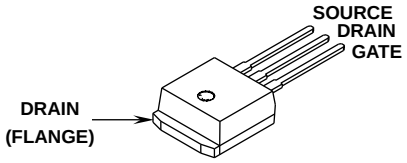
Formerly developmental type TA49027.

Packages

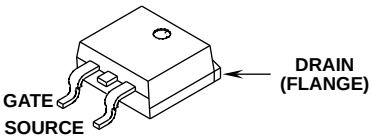
JEDEC TO-220AB



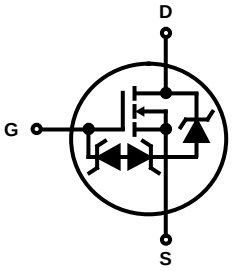
JEDEC TO-262AA



JEDEC TO-263AB



Symbol



Absolute Maximum Ratings $T_C = +25^oC$

	RFP30N06LE, RF1S30N06LE, RF1S30N06LESM	UNITS
Drain Source Voltage ..... V_{DSS}	60	V
Drain Gate Voltage ..... V_{DGR}	60	V
Gate Source Voltage ..... V_{GS}	+10, -8	V
Drain Current		
RMS Continuous ..... I_D	30	A
Pulsed Drain Current ..... I_{DM}	Refer to Peak Current Curve	
Pulsed Avalanche Rating ..... E_{AS}	Refer to UIS Curve	
Power Dissipation		
$T_C = +25^oC$ ..... P_D	96	W
Derate above $+25^oC$	0.645	$W/^oC$
Electrostatic Discharge Rating, MIL-STD-883, Category B(2) ..... ESD	2	kV
Operating and Storage Temperature ..... T_{STG}, T_J	-55 to +175	^oC
Soldering Temperature of Leads for 10s ..... T_L	260	^oC

File Number **3629.1**

Electrical Specifications $T_C = +25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu A$, $V_{GS} = 0V$		60	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 250\mu A$		1	-	2	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 60V$, $V_{GS} = 0V$	$T_C = +25^oC$	-	-	1	μA
			$T_C = +150^oC$	-	-	50	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = +10, -8V$		-	-	10	μA
On Resistance	$r_{DS(ON)}$	$I_D = 30A$, $V_{GS} = 5V$		-	-	0.047	Ω
Turn-On Time	t_{ON}	$V_{DD} = 30V$, $I_D = 30A$, $R_L = 1\Omega$, $V_{GS} = 5V$, $R_{GS} = 2.5\Omega$		-	-	140	ns
Turn-On Delay Time	$t_{D(ON)}$			-	11	-	ns
Rise Time	t_R			-	88	-	ns
Turn-Off Delay Time	$t_{D(OFF)}$			-	30	-	ns
Fall Time	t_F			-	40	-	ns
Turn-Off Time	t_{OFF}			-	-	100	ns
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 0V$ to $10V$	$V_{DD} = 48V$, $I_D = 30A$, $R_L = 1.6\Omega$	-	51	62	nC
Gate Charge at 5V	$Q_{G(5)}$	$V_{GS} = 0V$ to $5V$		-	28	34	nC
Threshold Gate Charge	$Q_{G(TH)}$	$V_{GS} = 0V$ to $1V$		-	1.8	2.6	nC
Input Capacitance	C_{ISS}	$V_{DS} = 25V$, $V_{GS} = 0V$, f = 1MHz		-	1350	-	pF
Output Capacitance	C_{OSS}			-	290	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	85	-	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$			-	-	1.55	$^oC/W$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$			-	-	80	$^oC/W$

Source-Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward Voltage	V_{SD}	$I_{SD} = 30A$	-	-	1.5	V
Reverse Recovery Time	t_{RR}	$I_{SD} = 30A$, $dI_{SD}/dt = 100A/\mu s$	-	-	125	ns

Typical Performance Curves

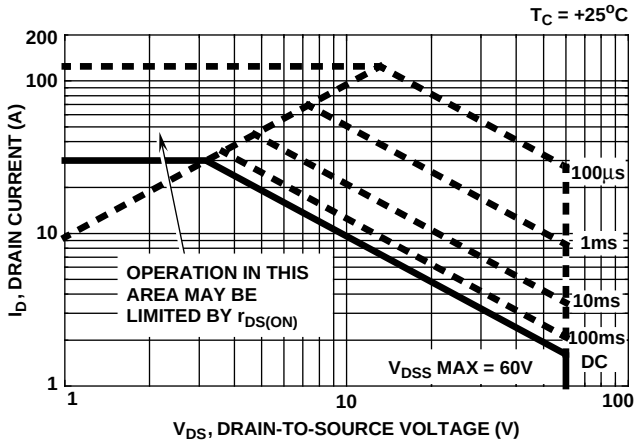


FIGURE 1. SAFE OPERATING AREA CURVE

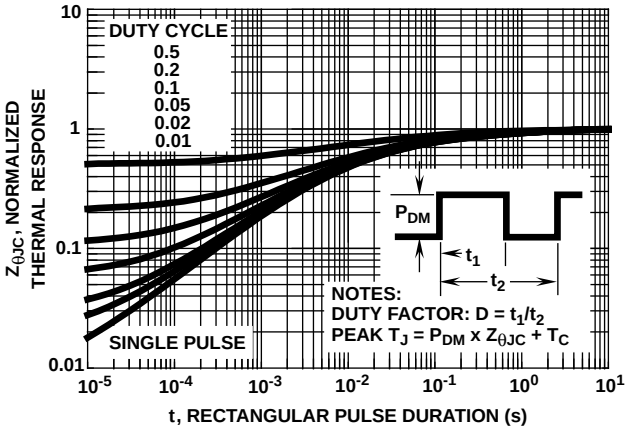


FIGURE 2. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

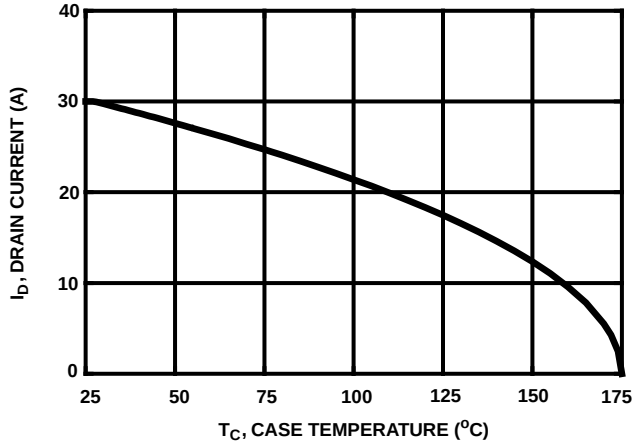


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

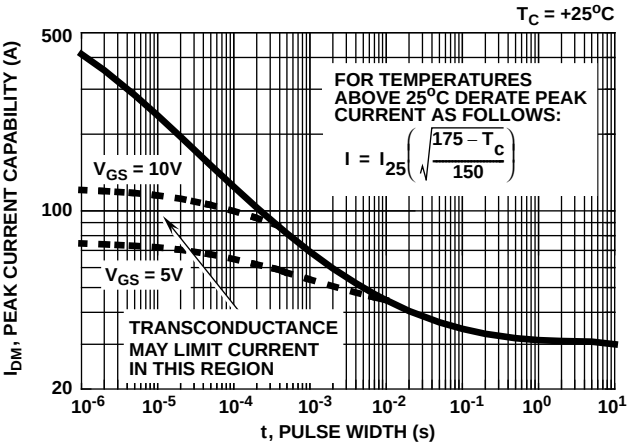


FIGURE 4. PEAK CURRENT CAPABILITY

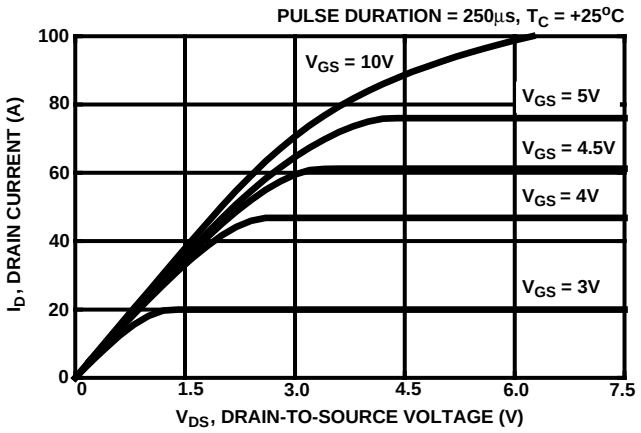


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

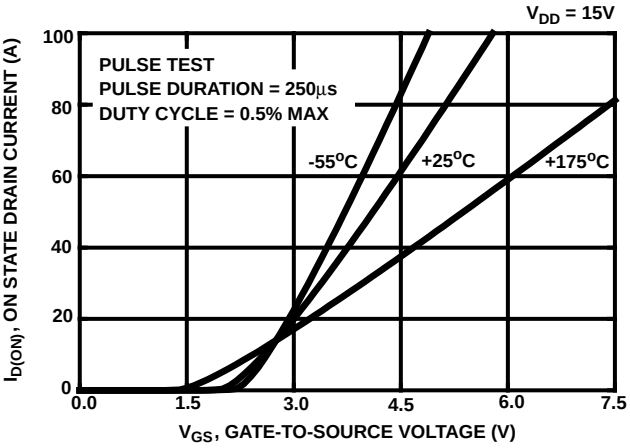


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

Typical Performance Curves (Continued)

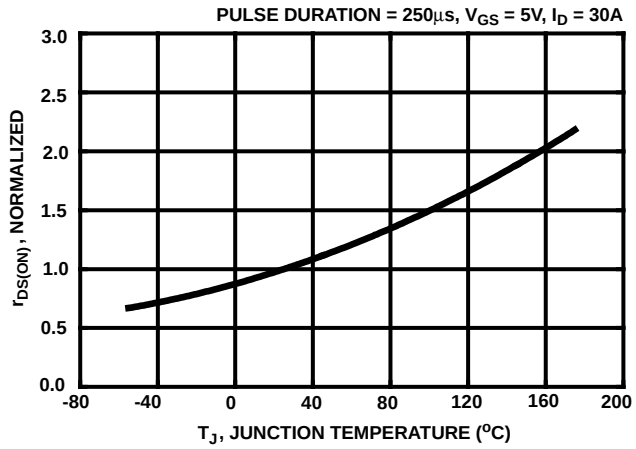


FIGURE 7. NORMALIZED $r_{DS(ON)}$ vs JUNCTION TEMPERATURE

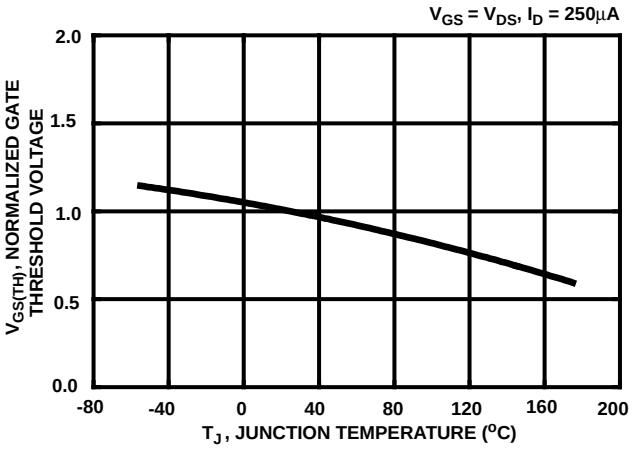


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs TEMPERATURE

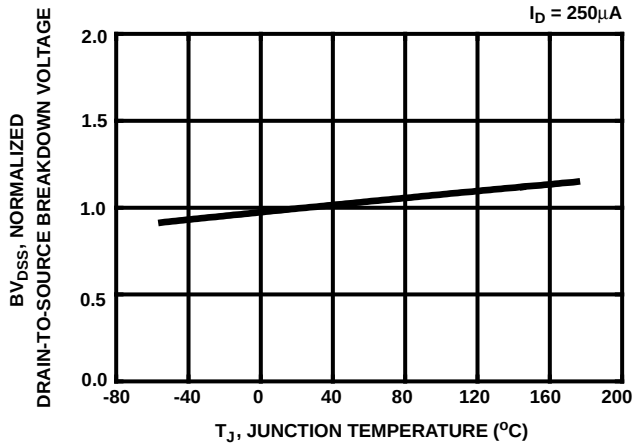


FIGURE 9. NORMALIZED DRAIN SOURCE BREAKDOWN VOLTAGE vs TEMPERATURE

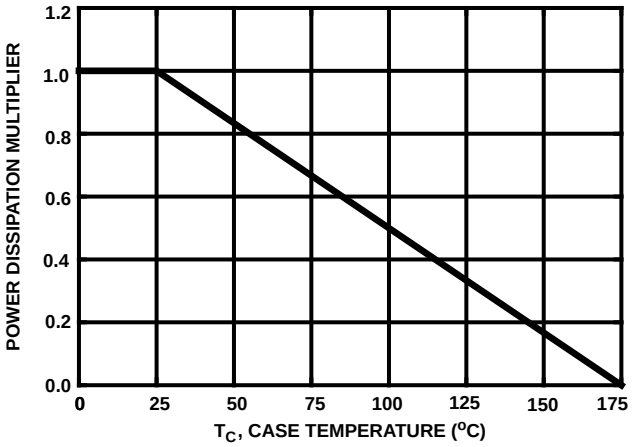


FIGURE 10. NORMALIZED POWER DISSIPATION vs TEMPERATURE DERATING CURVE

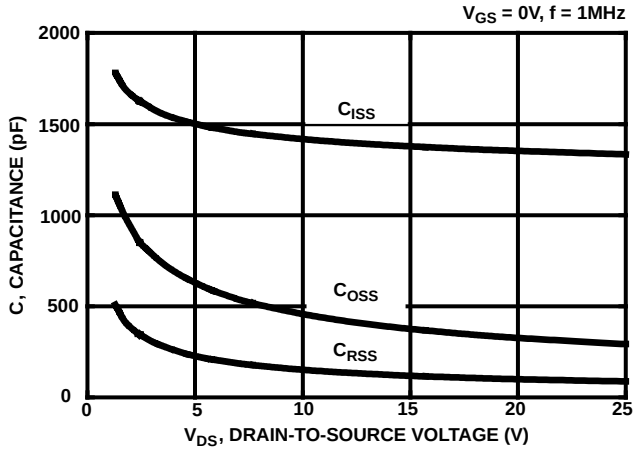


FIGURE 11. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

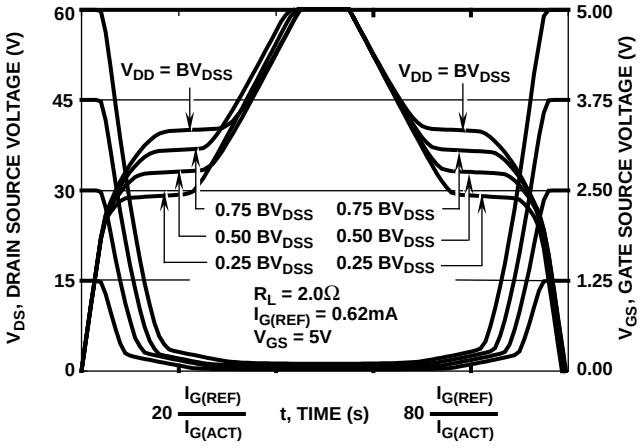


FIGURE 12. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT. REFER TO HARRIS APPLICATION NOTES AN7254 AND AN7260

Typical Performance Curves (Continued)

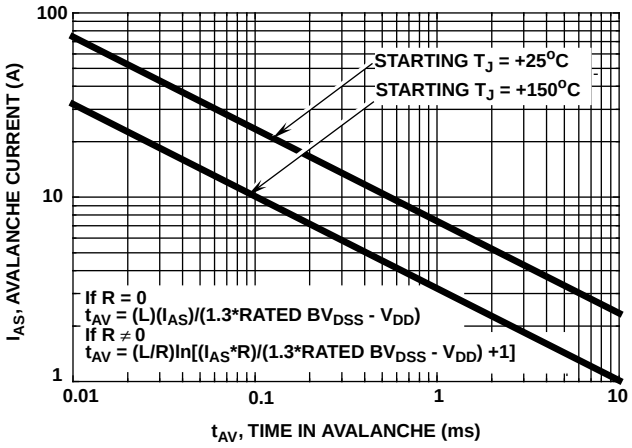


FIGURE 13. UNCLAMPED INDUCTIVE SWITCHING

Test Circuits and Waveforms

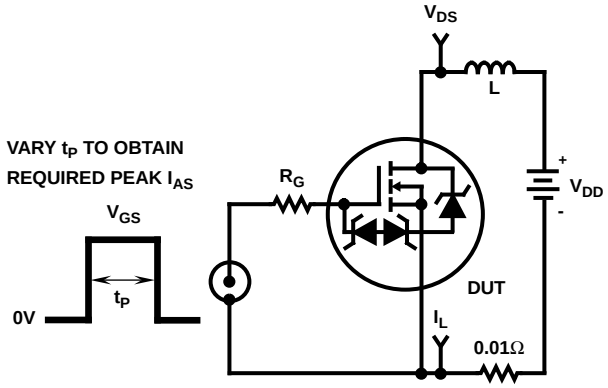


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

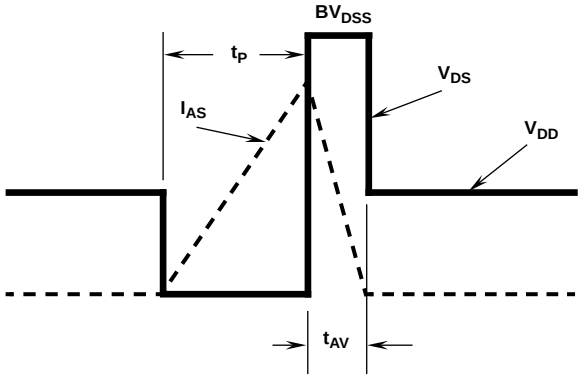


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

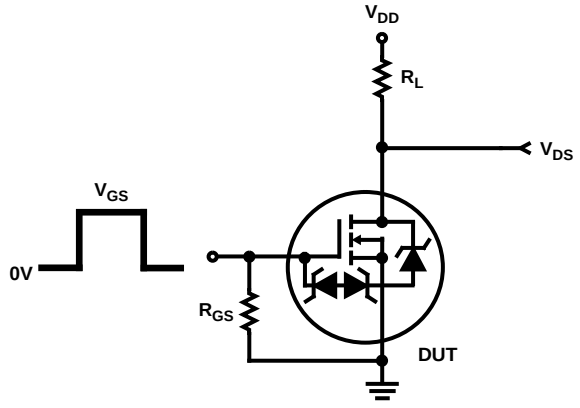


FIGURE 16. RESISTIVE SWITCHING TEST CIRCUIT

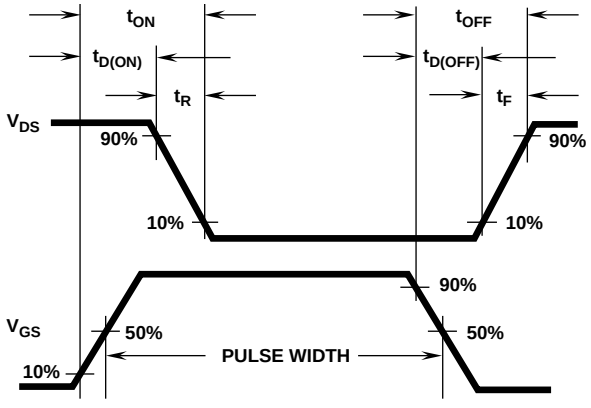


FIGURE 17. RESISTIVE SWITCHING WAVEFORMS

Temperature Compensated PSPICE Model for the RFP30N06LE, RF1S30N06LE, RF1S30N06LESM

```
SUBCKT RFP30N06LE  2 1 3;       rev 6/2/93
CA 12 8 1 3.34e-9
CB 15 14 3.44e-9
CIN 6 8 0 1.343e-9

DBODY 7  5  DBDMOD
DBREAK 5 11  DBKMOD
DESD1 91 9  DESD1MOD
DESD2 91 7 DESD2MOD
DPLCAP 10  5  DPLCAPMOD

EBREAK 11 7  17 18  75.39
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTO 20 6 18 8 1

IT 8 17 1

LDRAIN  2  5  1e-9
LGATE 1  9  7.22e-9
LSOURCE 3 7  6.31e-9

MOS1 16 6 8 8 MOSMOD M = 0.99
MOS2 16 21 8 8 MOSMOD M = 0.01

RBREAK 17 18 RBKMOD 1
RDRAIN 50 16 RDSMOD 11.86e-3
RGATE 9 20 2.52
RIN 6 8 1e9
RSCL1  5  51  RSLVCMOD 1e-6
RSCL2  5  50  1e3
RSOURCE 8 7 RDSMOD 26.6e-3
RVTO 18 19 RVTOMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 8 19 DC 1
VTO 21 6  0.5

ESCL  51 50  VALUE = {(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)*1e6/89,7))

.MODEL DBDMOD D (IS = 3.80e-13  RS = 1.12e-2  TRS1 = 1.61e-3  TRS2 = 6.08e-6  CJO = 1.05e-9  TT = 3.84e-8)
.MODEL DBKMOD D (RS = 1.82e-1  TRS1 = 7.50e-3  TRS2 = -4.0e-5)
.MODEL DESD1MOD D (BV = 13.54  TBV1 = 0  TBV2 = 0  RS = 45.5  TRS1 = 0  TRS2 = 0)
.MODEL DESD2MOD D (BV = 11.46  TBV1 = -7.576e-4  TBV2 = -3.0e-6  RS = 0  TRS1 = 0  TRS2 = 0)
.MODEL DPLCAPMOD D (CJO = 0.591e-9  IS = 1e-30  N = 10)
.MODEL MOSMOD NMOS (VTO = 1.94  KP = 139.2  IS = 1e-30  N = 10  TOX = 1  L = 1u  W = 1u)
.MODEL RBKMOD RES (TC1 = 1.07e-3  TC2 = -3.03e-7)
.MODEL RDSMOD RES (TC1 = 5.38e-3  TC2 = 1.64e-5)
.MODEL RSLVCMOD RES (TC1 = 1.75e-3  TC2 = 3.90e-6)
.MODEL RVTOMOD RES (TC1 = -2.15e-3  TC2 = -5.43e-6)
.MODEL S1AMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = -4.05  VOFF = -1.5)
.MODEL S1BMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = -1.5  VOFF = -4.05)
.MODEL S2AMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = -2.2  VOFF = 2.8)
.MODEL S2BMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = 2.8  VOFF = -2.2)

.ENDS
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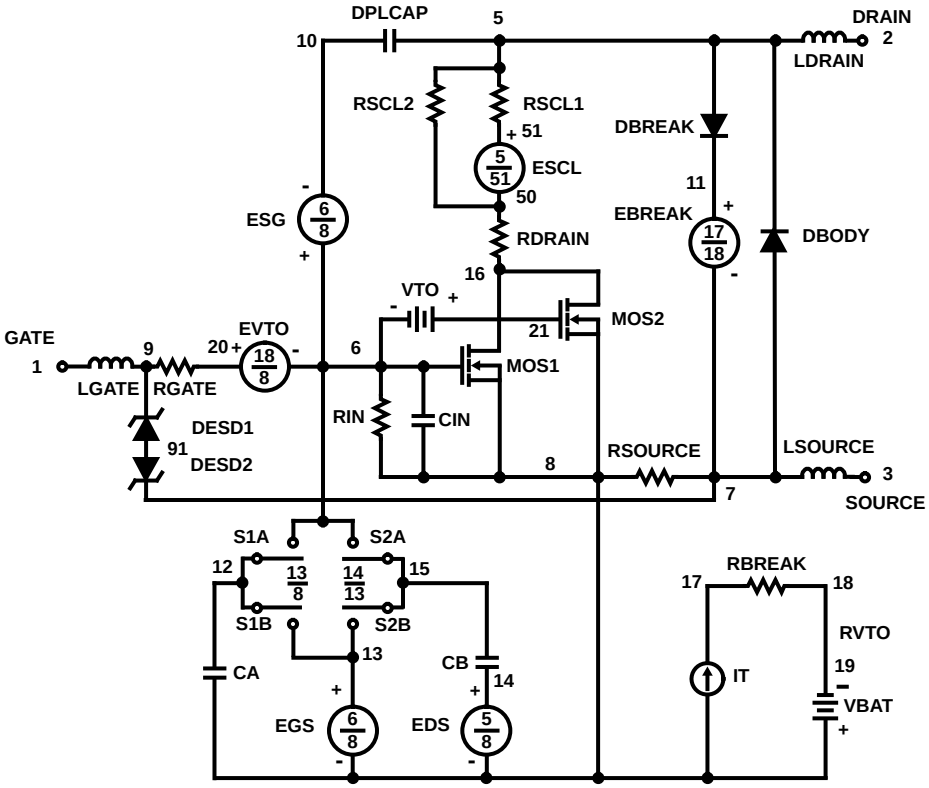

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records 1991.